CS-302 Quiz Preparation Virtual University

Sr	Questions	Answers Choice
1	Demultiplexer is also called.	A. Data selector B. Data router C. Data distributor D. Data encoder
2	LUT is acronym for _____.	A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options
3	Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state	A. Ten B. Eight C. Three D. Two
4	Demultiplexer converts _____ data to _____ data.	A. Parallel data, serial data B. Serial data, parallel data C. Encoded data, decoded data D. All of the given options
5	LUT is acronym for _____.	A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options
6	A positive edge-triggered flip-flop changes its state when _____	A. Low-to-high transition of clock B. High-to-low transition of clock C. Enable input (EN) is set D. Preset input (PRE) is set
7	_____ is one of the examples of asynchronous inputs.	A. J-K input B. S-R input C. D input D. Clear Input (CLR)
8	74HC163 has two enable input pins which are _____ and _____	A. ENP, ENT B. ENl, ENC C. ENP, ENC D. ENT, ENl
9	_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output	A. Resolution B. Accuracy C. Quantization D. Missing Code
10	In a state diagram, the transition from a current state to the next state is determined by	A. Current state and the inputs B. Current state and outputs C. Previous state and inputs D. Previous state and outputs
11	What is the difference between a D latch and a D flip-flop?	A. The D latch has a clock input B. The D flip-flop has an enable input C. The D latch is used for faster operation D. The D flip-flop has a clock input
12	Smallest unit of binary data is a _____	A. Bit B. Nibble C. Byte D. Word
13	A positive edge-triggered flip-flop changes its state when _____.	A. Low-to-high transition of clock B. High-to-low transition of clock C. Enable input (EN) is set D. Preset input (PRE) is set
14	Above is the circuit diagram of _____.	A. Asynchronous up-counter B. Asynchronous down-counter C. Synchronous up-counter D. Synchronous down-counter
		A. The next state of a given present state B. The previous state of a given

15	Given the state diagram of an up/down counter, we can find _____	present state C. Both the next and previous states of a given state D. The state diagram shows only the inputs/outputs of a given states
16	LUT is acronym for _____	A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options
17	74HC163 has two enable input pins which are _____ and _____	A. ENP, ENT B. ENl, ENC C. ENP, ENC D. ENT, ENl
18	LUT is acronym for _____	A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options
19	The design and implementation of synchronous counters start from _____	A. state table B. k-map C. state diagram D. Truth table
20	In asynchronous transmission when the transmission line is idle, _____	A. It is set to logic low B. It is set to logic high C. Remains in previous state D. State of transmission line is not used to start transmission